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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/617,026	07/11/2003	Seung-Woo Lee	6192.0302.US	2713

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EXAMINER	
MOON, SEOKYUN	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 06/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/617,026	LEE ET AL.	
	Examiner	Art Unit	
	Seokyun Moon	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1**, **2**, **4**, **7**, **10**, **11-18** is rejected under 35 U.S.C. 102(b) as being anticipated by Lien et al. (us. pat. no. 6,211,851 B1, herein after referred to as "Lien").

As to **claim 1**, Lien teaches a liquid crystal display comprising a liquid crystal panel assembly including a plurality of gate lines, a data line intersecting the gate lines, and a plurality of pixels (each of a plurality of pixels comprises a semiconductor switch as disclosed in col. 1 lines 37-40) connected to the gate lines and the data line [col. 1 lines 59-63] [col. 3 lines 61-65]. It should be noted that the Examiner cites the information from Lien's admitted prior art to meet the claim limitation since such LCD structure is standard, used widely, and is adopted in Lien's display device.

Lien further teaches the liquid crystal display comprising:

a gate driver [figs. 2 and 3] ("*gate driver 24*") sequentially scanning the gate lines by applying the gate voltage, each scanning being performed in a horizontal period including a first period (a part of the horizontal period occurred simultaneously with the period of applying a combined voltage of Vm and a data voltage to one of plural data lines, as shown in fig. 2) and a second period (a part of the horizontal period occurred simultaneously with the period of applying a signal data voltage to one of plural data lines, as shown in fig. 2) occurred following the first period;

a master data driver (the circuit embedded in Lien's driving circuitry supplying actual data voltage during the second portion of the scan data signal) [col.3 lines 39-41] sequentially applying data voltages selected from the gray voltages corresponding to the image data to the data line, each application is performed in the second period; and

a slave data driver (the circuit embedded in Lien's driving circuitry supplying a pre-charge level for upcoming data level) [col. 3 lines 39-41] applying the stored data voltage to the data line in each first period.

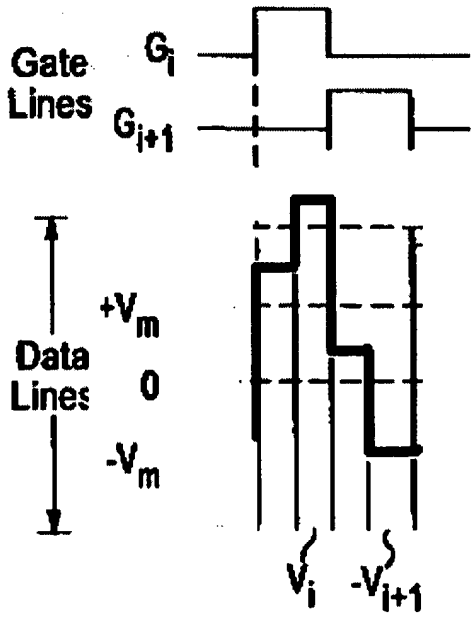
Lien [fig. 3] teaches a signal controller (the circuit supplying control signals for data driver and gate driver) receiving image data and a synchronization signal (""*data driver clock*" or "*clock line 26*") from an external device, processing the image data and generating control signals ("*data driver reset*", "*data driver enable*", "*gate driver enable*", ...) for displaying the image data;

Lien inherently teaches the slave data driver to store the data voltage applied to the data line in each second period of a scanning period since it is required for Lien to provide the opposite polarity of the previous data signal as a pre-charging signal in each

first period of the next scanning period and thus to require a device to store the previous data signal until the device applies the pre-charging signal in the next scanning period.

Lien inherently teaches a voltage generator generating a plurality of gray voltages and a gate voltage for driving the panel assembly since it is required for any type of liquid crystal device to apply gray scale voltage to pixels included in a display device to change the alignment of the liquid crystal display device to produce various gradations on a display and to apply a gate voltage to turn on the switching device included in a pixel, thus to allow the pixel to receive the data voltage.

As to **claim 2**, Lien teaches two data voltages sequentially applied to the data line have opposite polarity with respect to a predetermined voltage ("0V") [drawing 1 provided below] and the slave driver [fig. 3] inverts the polarity of the stored voltage before application to the data line [col. 5 lines 38-54].



Drawing 1

As to **claim 4**, most of the claim limitations have already been discussed with respect to the rejection of claims 1 and 2 except for the storage and the inverter being alternately connected to the data line.

The modified Lien [fig. 3] teaches the storage (included in the "*full frame buffer*", as discussed with respect to the rejection of claim 1) and the inverter ("*inverter 6*") alternatively connected to the data line ("*analog toggle 4*" alternatively connects the storage and the inverter to the data lines, as disclosed in col. 5 lines 40-49).

As to **claim 7**, Lien [fig. 3] teaches the slave driver to comprise a switch unit ("*analog toggle 4*") selectively connecting the storage (included in the "*full frame buffer*", as discussed with respect to the rejection of claim 1) and the inverter ("*inverter 6*") to the data lines [col. 5 lines 40-49].

As to **claim 10**, Lien [fig. 3] teaches the slave driver (the circuit embedded in Lien's driving circuitry supplying a pre-charge level for upcoming data level) [col. 3 lines 39-41] is formed on the panel assembly.

As to **claim 11**, Lien teaches the predetermined voltage being applied to the pixels [col.3 lines 29-41].

As to **claim 12**, Lien teaches a method of driving a liquid crystal display including first and second gate lines, a data line, a first pixel connected to the first gate line and the data line; and a second pixel connected to the second gate line and the data line as discussed with respect to the rejection of claim 1, the method comprising:

scanning the first gate line (during "*G1*" is high) [fig. 2];

applying a first data voltage ("*V1*") to the data line during the scanning of the first gate line;

applying the stored first data voltage ("*Vm-V1*" which is equal to "*-V1*" when "*Vm*" is equal to 0, as disclosed in col. 5 lines 25-27) to the data line during the scanning of the second gate line (during "*G2*" is high); and

applying a second data voltage ("*V2*") to the data line during the scanning of the second gate line (during "*G2*" is high).

Lien inherently teaches the method to comprise storing the first data voltage applied to the data line during the scanning of the first gate line since it is required for Lien to hold the first data voltage during the first horizontal period before the first data voltage is started to be applied to the data line during the second horizontal period as a pre-charging voltage.

As to **claim 13**, Lien [fig. 2] teaches inverting polarity of the stored first data voltage before the application of the stored first data voltage (applying "*-V1*" during second scanning period as a pre-charging voltage) [col. 5 lines 38-49].

As to **claim 14**, all of the claim limitations have already been discussed with respect to the rejection of claim 9.

As to **claim 15**, all of the claim limitations have already been discussed with respect to the rejection of claims 1 and 12.

As to **claim 16**, all of the claim limitations have already been discussed with respect to the rejection of claim 2.

As to **claim 17**, all of the claim limitations have already been discussed with respect to the rejection of claim 4.

As to **claim 18**, all of the claim limitations have already been discussed with respect to the rejection of claim 7.

4. **Claims 3** and **5** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lien in view of Washio et al. (us. pat. no. 6,873,313 B2, herein after referred to as "Washio").

As to **claim 3**, Lien does not teach expressly the master driver and the slave driver to be disposed at opposite sides of the panel assembly.

However, Washio [fig. 1] teaches a master driver ("*data signal line driving circuit SD*") and a slave driver ("*pre-charging circuit PC*") included in an image display device and disposed at the opposite sides of the panel.

It would have been obvious to one of ordinary skill in the art at the time of the invention to place Lien's master driver and the slave driver separately at opposite sides of the panel, as taught by Washio, to distribute the driving circuitry into the sides of the display, thus to provide more space in the center of the display.

As to **claim 5**, Lien does expressly disclose the storage to comprise a capacitor.

However, Washio [figs. 1 and 3] teaches an image display device having a pre-charging unit (a combination of "*pre-charging circuit PC*" and "*pre-charging voltage stabilizing section ST*") comprising a capacitor ("*charging holding means*" shown in fig. 3) to store a pre-charge voltage ("*PCV*") [col. 12 lines 1-20].

It would have been obvious to one of ordinary skill in the art at the time of the invention to define Lien's storage to comprise a capacitor rather than any other electrical components capable of storing, as taught by Washio, since capacitor is well known for low cost and is widely used in a driving circuitry for a display.

5. **Claim 6** is rejected under 35 U.S.C. 103(a) as being unpatentable over Lien in view of Lautzenhiser (us. pub. no. 2002/0149503 A1, herein after referred to as "Lautzenhiser").

Lien [fig. 3] teaches an inverter ("*inverter 6*") included in a driving circuitry.

Lien does not expressly disclose the specific structure of the inverter included in the display driving circuitry.

However, Lautzenhiser [fig. 21] discloses an inverter ("*inverter 350*") comprising an operation amplifier ("*operational amplifier 354*") in a negative feedback configuration having a non-inverting input terminal supplied with the predetermined voltage ("*ground*") [par. (0223)].

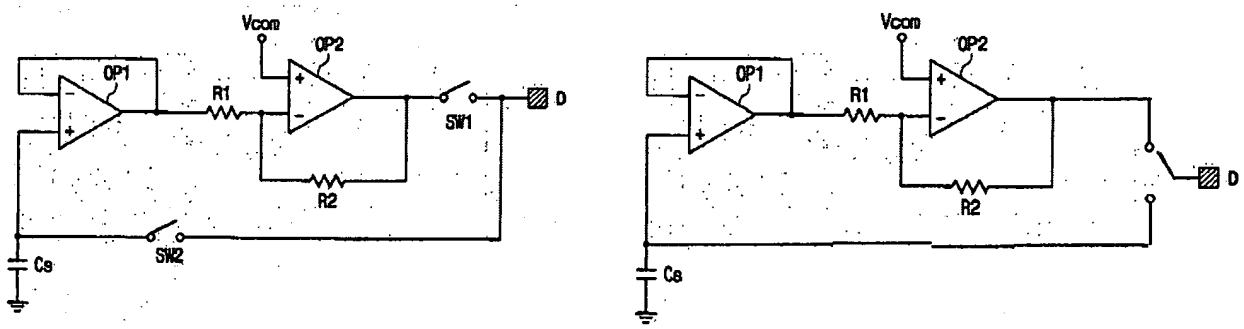
It would have been obvious to one of ordinary skill in the art at the time of the invention to specify the internal structure of Lien's inverter in such way, as taught by Lautzenhiser, since including an operation amplifier in a negative feedback configuration to implement an inverter is well known and widely used in electronic circuit design.

6. **Claims 8**, **9** and **19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lien.

As to **claim 8**, Lien does not teach expressly the switch unit to comprise a first switch and a second switch.

However, since applicant has failed to disclose that having two switches in the switch unit provides an advantage, is used for particular purpose, or solves a state problem, it is an obvious matter of design choice to include two switches in the switching unit.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a toggle switch for the switching operation of the driver, since a toggle switch would perform equally well at selectively connecting inputs from the storage and the inverter to the data line. Drawing 2 is provided below to illustrate an alternative structure for the switching unit.



Design I Design II

Drawing 2

As to **claim 9**, Lien teaches the slave driver (the circuit embedded in Lien's driving circuitry supplying a pre-charge level for upcoming data level) [col. 3 lines 39-41] to comprise a buffer ("*full frame buffer*") [fig. 3] for buffering the data voltage ("*D1*", "*D2*",

"*D3*", ...) stored in the storage and provides the buffered data voltage for the inverter ("*inverter 6*") [col. 5 lines 38-49].

Lien does not expressly disclose the buffer to include an operational amplifier.

However, Examiner takes official notice that using an operational amplifier for a buffer is widely known and used.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to specify Lien to adopt an operational amplifier as its buffer.

As to **claim 19**, all of the claim limitations have already been discussed with respect to the rejection of claim 8.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Liaw (us. pat. no. 6,483,494, B1) teaches a multistage charging circuit for driving liquid crystal displays, designed particularly to provide a multi-stage charging driving circuit for liquid crystal display, in which the pixels can be pre-charged to a determined voltage value before the next data are written by performing charge-sharing and pre-charge.

Kim (us. pub. no. 2003/003876 A1) teaches an apparatus and method for driving an electro-luminescence panel wherein pixels in a current driving type electrode-luminescence panel are pre-charged to change a storage voltage of the pixel into the corresponding voltage within a limited scanning time.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Seokyun Moon whose telephone number is (571) 272-5552. The examiner can normally be reached on Mon - Fri (8:30 a.m. - 5:00 p.m.).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

May 24, 2006
S.M.

KENT CHANG
PRIMARY EXAMINER